Charge Overflow Control of A 3.96-µm 124dB HDR-DPS for Triple and Single Quantization Dual-Channel Operation

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ABSTRACT

In this paper, a dual-channel triple-quantization digital-pixel-sensor (3Q-DPS) [1], [2] which simultaneously captures a 124 dB high dynamic range (HDR) visible-light image and a 60 dB dynamic range (DR) near-infrared (NIR) depth image in global shutter is described. The sensor architecture and basic operation have already been reported [3], [4], and the charge overflow control technology of the shared floating diffusion (FD) 3Q-DPS will be presented in this paper. Specifically, asymmetric one-side buried overflow paths are developed to prevent charge mixing in FD and charge leakage to the drain. The design was studied with an analytical model and Technology Computer Aided Design (TCAD) simulation which is verified with measurements. With this overflow control, good photo-response linearity without charge mixing or charge loss is achieved in the dual-channel operation.

I. INTRODUCTION

A 127 dB HDR global shutter CMOS image sensor with 3Q-HDR readout by the overflow charge accumulation in FD and in-pixel analog-to-digital conversion has been reported [1], [2]. Moreover, a dual-channel 3Q-DPS, which has visible-sensitive photodiode (PD) with a large micro-lens capable of the 3Q-HDR readout and NIR-sensitive PD with a small micro-lens operating in the conventional 4-transistor (4T) correlated double sampling (CDS) readout has been reported [3], [4]. Its simultaneous capture of an HDR visible-light image and an NIR depth image in global shutter is effective for small form-factor augmented reality and virtual reality (AR/VR) devices.

II. TRIPLE QUANTIZATION OPERATION

Fig. 1 shows the concept of the 3Q-HDR operation. Under the very high illuminance, the excess charges above PD saturation level overflow to the FD and in-pixel charge accumulation capacitor, C_S. During exposure, the FD node potential is compared to the reference level (V_{FD_REF}) by the in-pixel comparator. When the FD node potential is decreased by the overflow charges and reaches V_{FD_REF}, the comparator output is flipped, and the time code is stored in the in-pixel memory. This saturation time detecting operation is known as time-to-saturation (TTS), and its effective signal charge is extended as

$$Q_{EQ\_TTS} = \frac{N_{max}}{N_{flip}}\{Q_{PDFWC} + (C_{FD} + C_S) \times \Delta V_{TTS}\} \quad (1)$$

where, N_{max}, N_{flip}, Q_{PDFWC}, C_{FD}, C_S, and ΔV_{TTS} are the maximum time code, the flipped time code, PDFWC, FD capacitance, charge accumulation capacitance, and voltage swing of the TTS. The lateral overflow integration capacitor (LOFIC) [5] operation, which is a combination of the 4T-CDS readout with only the charges accumulated in PD and low conversion gain 3T readout with the charges accumulated in PD and FD, is also applied to the low and middle illuminance conditions to maintain the same low light performance as conventional 4T pixel CMOS image sensors.

Therefore, one of the key requirements to realize this 3Q-HDR operation is sufficient charge overflow capability from PD to FD to accumulate them in the FD node. In this paper, the charge overflow integration capability and the 3Q-HDR pixel design are described.

III. DUAL-CHANNEL OPERATION

Fig. 2 shows a conceptual diagram of the dual-channel 3Q-DPS [3], [4]. The sensor captures the visible and NIR depth images in the same frame. In AR/VR glasses, higher DR is required, especially in the visible channel, because the brightness of the scene could vary significantly.

Fig. 3 shows a stacked pixel structure. Two visible-sensitive PDs (MONO-PD) and NIR-sensitive PDs (NIR-PD) are diagonally arranged in a 3.96µm FD-shared super-pixel.

Fig. 4 shows the super-pixel circuit diagram and the operation timing of the dual-channel 3Q-DPS. FD, source follower (SF) amplifier, a comparator, and dual-bank static random access memory (SRAM) are shared by the 4 PDs. The dual-bank 10-bit SRAMs are implemented in each super-pixel to store the dual-channel output signals in global sampling to realize global shutter operation. In this sensor, HDR is realized in the MONO-PD readout by the developed 3Q-HDR technology, and good low noise performance is realized in the NIR-PD by the conventional 4T CDS readout.

IV. OVERFLOW CONTROL

The charge overflow control is the most critical requirement for the dual-channel operation with 3Q-HDR readout of the MONO PD. In the MONO-PD, the excess charges above PD saturation must overflow from PD to FD to realize charge accumulation in FD. On the other hand, in the NIR-PD, the excess charges must overflow to the overflow drain (OFD) to prevent charge mixing with the overflow charges from the MONO-PD in FD. The desired charge overflow direction of each PD is illustrated in Fig. 5.

The relation between the overflow error R_{err} and the overflow barrier heights can be formulated by a simple model shown in Fig. 6. The overflow currents from MONO-PD to FD (I_{of}) and OFD (I_{err}) are expressed as

$$I_{of} = I_0 e^{-\frac{q\Phi_B}{nkT}} \tag{2}$$

$$I_{err} = I_0 e^{-\frac{q\Phi_B{}'}{nkT}} \tag{3}$$

where, Φ_B, $\Phi_B{}'$, I_0, n, q, k, and T are the overflow barrier height of the FD and OFD directions, overflow current at $\Phi_B = 0$, ideality factor, the elementary charge, Boltzmann constant, and temperature, respectively.

The overflow error R_{err} is defined as the ratio of the error and proper overflow currents in equation (4) below.

$$R_{err} = \frac{I_{err}}{I_{of}} = \frac{e^{-\frac{q\Phi_B{}'}{nkT}}}{e^{-\frac{q\Phi_B}{nkT}}} = e^{-\frac{q(\Phi_B{}'-\Phi_B)}{nkT}} = e^{-\frac{q\Delta\Phi_B}{nkT}} \tag{4}$$

Then, the relation between the overflow barrier difference $\Delta\Phi_B = \Phi_B{}' - \Phi_B$ and R_{err} is calculated as

$$\Delta\Phi_B = \frac{nkT}{q}\ln\frac{1}{R_{err}} \tag{5}$$

For example, the calculation result of $\Delta\Phi_B = 120mV$ is obtained by (5), when $R_{err} = 0.01$ (=-40 dB), $n = 1$, and $T = 300K$ are assumed.

The relation between R_{err} and $\Delta\Phi_B$ calculated from (5) is shown in Fig. 7. To achieve the target $\Delta\Phi_B$, the asymmetric one-side buried overflow path [6]-[9] is formed as shown in Fig. 7, realizing robust overflow control and dark current suppression under the gates.

V. TCAD SIMULATION

Fig. 8 shows the pixel cross-section and the TCAD simulation condition for the asymmetric overflow pixel design. A negative supply voltage is applied to all TGs and ABs to suppress the dark current generated at the Si surface under them [9]-[12]. Although the negative bias makes the overflow potential barrier increase, sufficient overflow barrier difference $\Delta\Phi_B$ is formed by the developed asymmetric one-side buried overflow path technology.

In this pixel simulation and design, $\Delta\Phi_B$ is varied by the different n-type implant dosage of the buried overflow path. The FD and OFD nodes are connected to the VAAPIX in this simulation.

VI. EXPERIMENTAL VALIDATION

Fig. 9 shows the fabricated chip micrograph and the specifications. Figs. 10 and 11 show the measurement timing and the results of the overflow error, respectively. In the MONO-PD, the condition of 100 % overflow is defined as the measured slope with always-high TG during exposure. On the other hand, in the NIR-PD, the condition of 0 % overflow error is defined as the measured slope with always-high AB. By comparing the normal operation slope and these slopes, as shown in Fig. 10, R_{err} is calculated. The FD parasitic light sensitivity (FD PLS) is removed by the calculation. Negative voltage is supplied to all the TGs and ABs during exposure.

Three wafers which have different n-type implant conditions of the asymmetric overflow path are fabricated. The results of Fig. 11 agree well with the TCAD simulation result and the analytical model of (5).

Fig. 12 shows the photo-response curves of the MONO-PD and NIR-PD after linearization signal processing. Even under the high illuminance, a good linearity without charge mixing at the FD or charge loss drained by OFD is achieved with the developed asymmetric overflow mechanism.

Fig. 13 shows the quantum efficiency of the dual-channel global shutter output signals. Good visible and NIR sensitivity has been obtained in a single frame capture.

Table 1 shows the performance comparison between the latest DPSs. This dual-channel 3Q-DPS has extremely higher DR of over 120 dB in 3.96 μm super pixel. Moreover, the dual-channel 3Q-DPS operation, which captures the visible image and the NIR depth image simultaneously in global shutter, has been demonstrated without any degradations of linearity.

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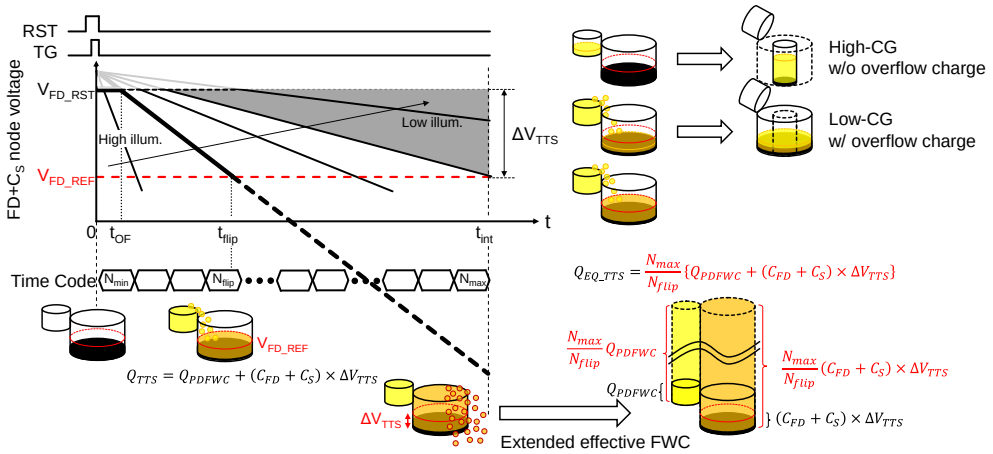


Fig. 1 Concept of 3Q-HDR operation.

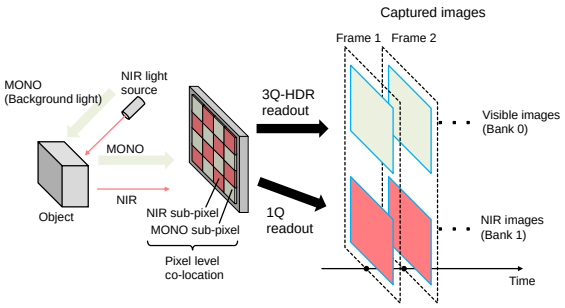


Fig. 2 Concept of dual-channel 3Q-DPS.

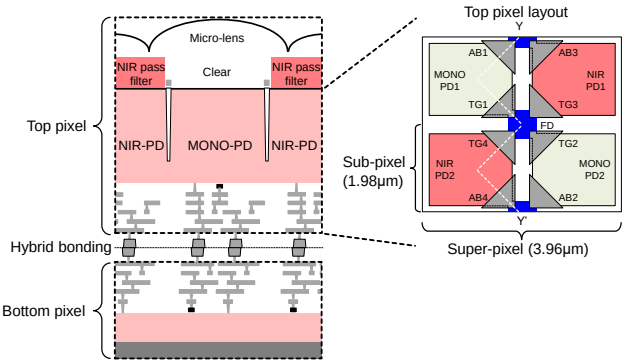
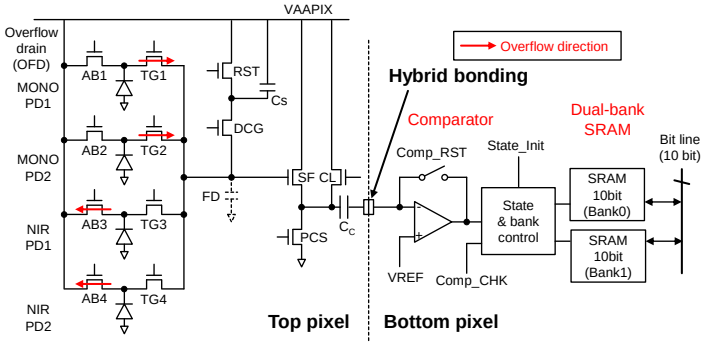
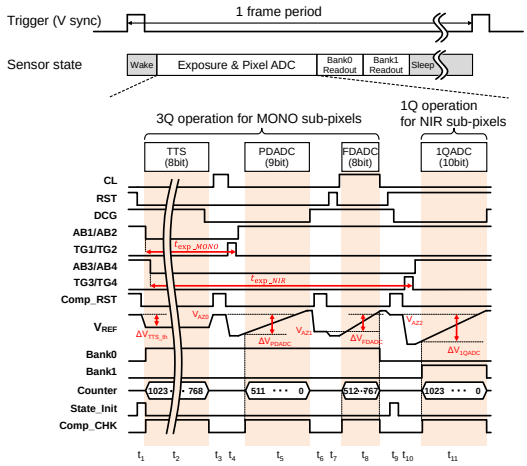


Fig. 3 Stacked pixel structure of dual-channel 3Q-DPS.



(a) Stacked dual-channel 3Q-DPS pixel schematic.



(b) Operation timing.

Fig. 4 Stacked pixel schematic and operation timing of dual-channel 3Q-DPS.

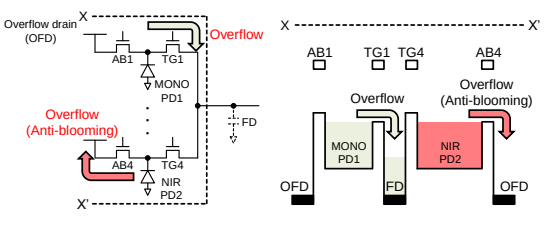


Fig. 5 Required overflow control.

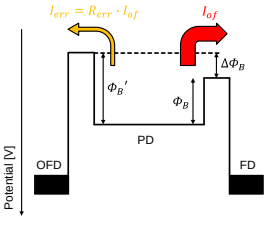


Fig. 6 Analytical model.

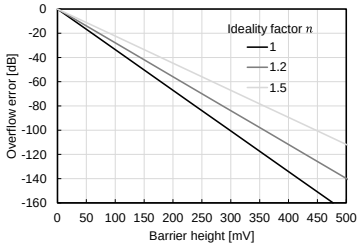


Fig. 7 Barrier height and overflow error.

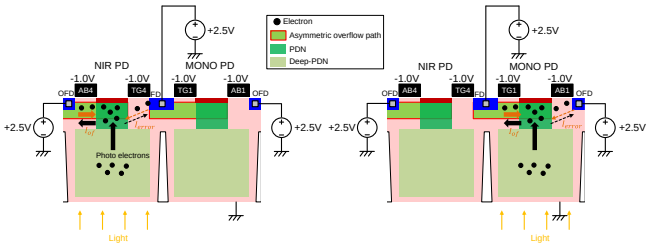
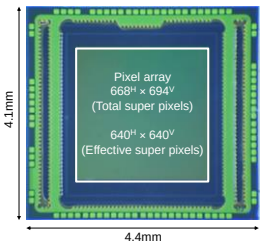
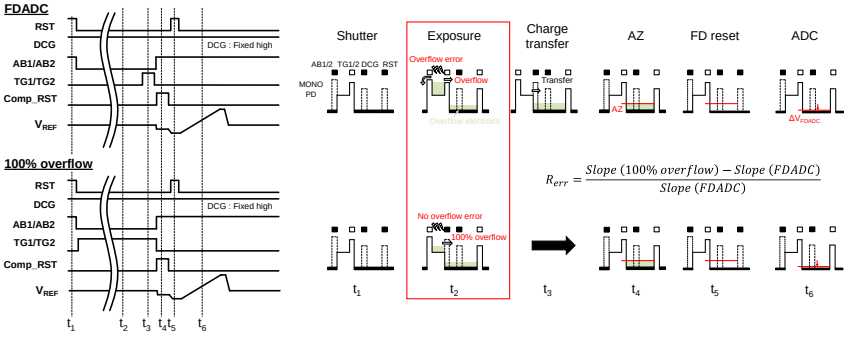


Fig. 8 Pixel structure and TCAD simulation condition.

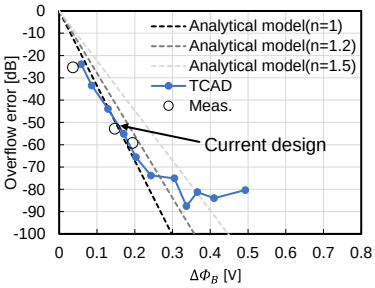


Specifications	
Process	45nm/40nm
Super pixel size	3.96μm^{H} × 3.96μm^{V}
Sub pixel size	1.98μm^{H} × 1.98μm^{V}
Chip size	4.4mm^{H} × 4.1mm^{V}
# of pixels	640^{H} × 640^{V}

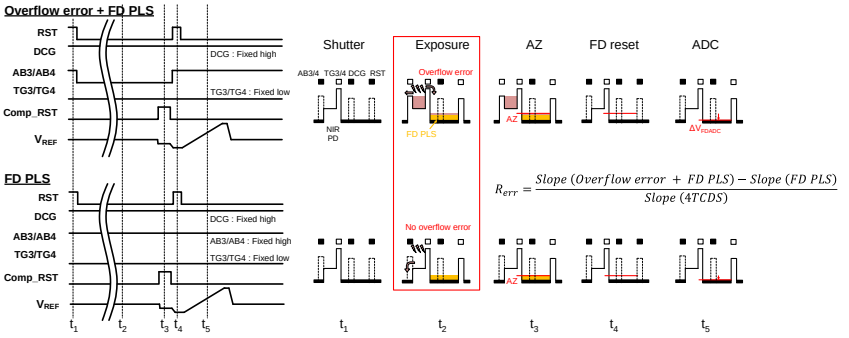
Fig. 9 Chip micrograph and specifications.



(a) MONO-PD.

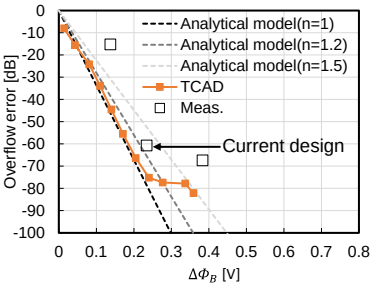


(a) MONO-PD.



(b) NIR-PD.

Fig. 10 Timing diagram for overflow error measurement.



(b) NIR-PD.

Fig. 11 Measured overflow error.

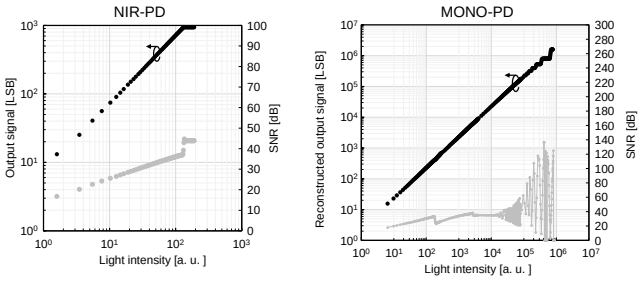


Fig. 12 Measured photo-response curves.

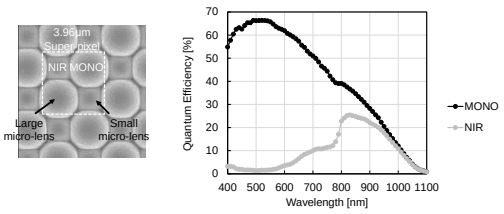


Fig. 13 Measured quantum efficiency.

Table 1 Performance comparison of the latest DPS.

Specification	This work		SSCL2024 [13]	TED2022 [2]	JSSC2022 [14]	JSSC2018 [15]
	MONO-PD	NIR-PD				
Process technology	45nm/40nm		65nm/40nm	45nm/65nm	65nm/28nm	90nm/65nm
Pixel size [μm]	**3.96**		6.3	4.6	4.95	6.9
# of pixels (H x V)	640×640		640×480	512×512	1668×1364	1632×896
Dual-channel capture	**Yes**		No	No	Possible	No
Pixel memory	**10b×2**		10b	10b	22b	15b
QE (@530/940nm) [%]	**66/22**	**1.6/19**	NA	96/41	NA/NA	NA/NA
Dynamic range [dB]	**124**	60	120	127	84*	70.2
Linear full well [ke$^-$]	**3234 (TTS)**	6.3	11000*	9000 (TTS)	38	16.6 (Saturation)
Noise floor [e$^-$]	6.3 (w/o FPN cancel) 6.4(w FPN cancel)		11	4.2	2.45 (24dB gain)	5.15
Power [mW]	6.2		1.33	5.75	116.2(30fps)	746 (660fps)
Overflow error [dB]	**-53**	**-61**	N/A	N/A	N/A	N/A

* : Calculated from the relation between DR, LFWC, and noise floor